REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Status of Claims:

Claims 1, 3-7, 9-12 are amended. Claims 1-12 are presented for examination.

Objections to the Specification:

In paragraph 2-3 of the office action, the Examiner objected to informalities in the specification. Per the Examiner's suggestion, the paragraph starting at page 2 line 16 has been amended.

Claim Objections and 35 U.S.C. 112 Rejections:

Claims 1, 3-7, and 9-12 are objected to for having informalities. Claims 3-7 and 9-12 are rejected under 35 U.S.C. 112, second paragraph.

In light of the current amendments, the above-referenced objections and rejections to claims 1, 3-7, and 9-12 are respectfully traversed.

The claims objected to in paragraphs 4-8 of the office action have been amended based on the Examiner's suggestions. In claim 1, the term "said approximate expression" is amended to "said corrected approximate expression." In claims 3-5, 9-12, the terms "the reciprocal" are amended to "a reciprocal." In claims 4, 6, 10, and 12, the term "dividing the range" are amended to "dividing a range". In claim 7, the term "the diffusion length dependence" is amended to "a diffusion length dependence."

For claims 4, 6, 10, and 12, the examiner rejected these claims based on 35 U.S.C. 112 for being unclear (regarding "selectively applied") and indefinite (regarding "plurality of ranges"). As amended, claim 4 now recites that "<u>each of said plurality of polynomials applied to one of a plurality of diffusion length ranges</u> obtained by dividing a range of diffusion length values by one or more predetermined approximate critical diffusion length values." (Emphasis added.) The amendments are fully supported by the specification, which describes

dividing a range of diffusion length values based on a critical value (DLC), and applying a different polynomial to each range. (Specification; page 17 line 18 – page 18 line 17; Fig. 7C, ranges L3, L4.) Claims 6, 10, and 12 are amended similarly as claim 4.

For claims 3-6 and 9-12, the terms "the diffusion-length-dependent approximate expression" are amended to "the corrected approximate expression."

For claims 7, the term "the correction values" is amended to "correction values".

In light of these amendments, it is thus submitted that claims 1, 3-7, and 9-12 fully satisfy the requirements of 35 U.S.C. 112, second paragraph.

Prior Art Rejections:

Claims 1, 2, 7, and 8 are rejected under 35 U.S.C. 102(a) as being unpatentable over Chung et al ("An Analytical Threshold-Voltage Model of Trench-Isolated MOS Devices with Nonuniformly Doped Substrates", IEEE Transactions on Electron Devices, Vol. 39, No. 3, March 1992) (hereinafter Chung) in view of Zhang et al (U.S. Patent No. 6,618,837). Claims 3, 4, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung and Zhang, and further in view of Lin et al ("A Closed-Form Back-Gate-Bias Related Inverse Narrow-Channel Effect Model for Deep-Submicron VLSI CMOS Devices Using Shallow Trench Isolation", IEEE Transactions on Electron Devices, Vol. 47, No. 4, April 2000) (hereinafter Lin).

With respect to claims 1-4 and 7-10, the above-referenced rejections are respectfully traversed.

As amended, claim 1 recites a circuit simulation apparatus with the features of:

> "a simulation executing unit which reads a circuit net list in which the connection descriptions of a circuit to be simulated are stored and which calculates the changes in the current and voltage of said circuit to be simulated, by referring to a transistor model, and
>
> <u>a diffusion-length-dependent parameter correcting unit</u> which creates a corrected approximate expression regarding a

diffusion-length-dependent parameter whose values change depending on <u>a diffusion length of a transistor</u> for a transistor model created on the basis of transistors having a predetermined diffusion length and which calculates the correction value of said diffusion-length-dependent parameter for a transistor model having the diffusion length different from that of said transistor model by using said corrected approximate expression,

<u>wherein said transistor includes a source region and a drain region, and an isolation region surrounds said source region and drain region, and</u>

<u>wherein said diffusion length of said transistor is defined by a distance between boundaries of said isolation region in a direction from the source region to the drain region</u>."

The circuit simulation apparatus of claim 1 has at least the advantage that it simulates the performance of a circuit netlist taking into account the diffusion lengths (DL) of the transistors, thus achieving improvements in simulation accuracy. (Specification, page 5, lines 3-11.) As explained in the specification, the diffusion length of a transistor affects the transistor performance because the carrier mobility is affected by the deformation caused by surrounding STI (shallow trench isolation) regions. (Specification, page 11 line 8 – page 12 line 2.)

As illustrated in Figs. 2A and 2B, as well as the corresponding specification text (page 3, lines 4-25), the diffusion length (DL) of a transistor is defined by the boundaries of two neighboring STI (shallow trench isolation) regions <u>in a direction perpendicular to the gate electrode</u> (32 or 46). In the planar view of Fig. 2A, the diffusion length (DL) is the length of the field region 31 in a direction perpendicular to the gate electrode 32 annotated as "DL". In the corresponding sectional view of Fig. 2B, the diffusion length (DL) equivalent to that in 2A is the distance between the right edge of the left STI region 47 and the left edge of the right STI region 47. The specification describes the diffusion length as "the total length of the source length, channel length and drain length." (Specification, page 3, lines 10-12.)

It is well known to those skilled in the art of MOS device simulation that the channel length (or transistor gate length) of a MOS transistor is the distance between the edges of the

LDD regions (elements 44 in Fig. 2B). Thus, when a transistor is "on", a depletion region forms under the gate electrode (element 46 in Fig. 2B), forming a conductive path between the source region and drain region (elements 43, 44 in Fig. 2B). Hence, it is also well known to those skilled in the art that a reference to a "length" of a transistor refers to a distance in a direction parallel to the current flow direction (e.g., a direction perpendicular to the gate electrode). Similarly, it is also well know to those skilled in the art that a "width" of a transistor refers to a distance in a direction perpendicular to the current flow direction (e.g., a direction parallel to the gate electrode). The current application uses the description "length" consistent with standard terminology, as evidenced by the "DL" annotated in Fig. 2A running perpendicular to the gate electrode 32.

It is well known to those skilled in the art that the channel length and the channel width of a transistor affects its electrical performance. These are known as short-channel effects and narrow-channel effects, respectively. The applicant acknowledges these effects in the discussion of background art. (See specification, page 2, lines 1-7.) In addition to these effects, the circuit simulation apparatus of claim 1 takes into account <u>the diffusion length</u> of a transistor for calculation of diffusion-length-dependent parameters, in order to achieve a more accurate simulation. As explained in the specification, the diffusion length of a transistor is a sum of the total lengths of the source length, channel length, and drain length. (Specification, page 3, lines 9-12.)

By contrast, Chung does not describe modeling transistor performance based on a <u>diffusion length</u> of a transistor, but describes a relationship based on the <u>width (W)</u> of the transistor. (Chung, col. 1, paragraph 1, "as the channel width is reduced, this effect will cause a reduction of the threshold voltage ..."). For example, equation 8 of Chung describes the model relationship between the Vt (threshold voltage) and W (channel width). The Chung reference uses the term "width" consistently with industry standard terminology. In Fig. 1 of Chung, the width (Wm) direction of the transistor is defined in a direction perpendicular to the source-to-drain direction. (Chung, Fig. 1, Wm indicated in the "Z" direction, whereas source-to-drain indicated in the "Y" direction.) The discussions, figures, and equations in Chung all direct at a <u>channel-width dependency</u> of transistor performance, with no mention of

the overall diffusion length as defined in the current application. (The diffusion length being the sum of the channel length, source lengths, and drain lengths.)

The deficiencies of Chung cannot be cured with Zhang or Lin because neither Zhang nor Lin discusses using diffusion length in transistor simulation. For example, the Lin reference also discusses a channel-width dependency of transistor performance. (See Lin; title, abstract, introduction.) In Lin, the figures illustrate that its use of the term "width" also conforms with industry standard terminology. The cross-sectional image and figure shown in Figs. 1-2 of Lin is clearly across the width-direction of a transistor because the source/drain regions are not visible in the pictures. (The source/drain regions are visible only along a cross-section in the length-direction of a transistor, as illustrated in Figs. 2A and 2B of the current application.) Hence, the width discussed in Lin clearly differs from the diffusion length discussed in the current application, because the width does not include the components of channel length, source length, and drain length.

Because the specification of the current application clearly defines diffusion length, it is believed that the original claim 1 is allowable over the cited references of Chung and Zhang. However, to further clarify claim 1 and distinguish over the cited references, claim 1 is amended to include "wherein said transistor includes a source region and a drain region, and an isolation region surrounds said source region and drain region, and wherein said diffusion length of said transistor is defined by a distance between boundaries of said isolation region in a direction from the source region to the drain region." This limitation is clearly supported by the text. (See application; page 3, lines 4-25; Figs. 2A-2B.)

Therefore, it is submitted that amended claim 1 is allowable over the cited references. Claims 2-4 are dependent claims of claim 1, and therefore are allowable for at least the same reasons as those stated for claim 1.

Claim 7 recites a transistor model creating method with similar features as the apparatus claim of claim 1. Claim 7 has also been amended to include "wherein said transistor includes a source region and a drain region, and an isolation region surrounds said source region and drain region, and wherein said diffusion length of said transistor is defined

by a distance between boundaries of said isolation region in a direction from the source region to the drain region." Therefore, claim 7 is allowable for substantially the same reasons as those of claim 1. Claims 8-10 are dependent claims of claim 7, and therefore are deemed allowable as well.

Allowable Subject Matter:

The applicant appreciates the indication that claims 5, 6, 11, and 12 are allowable if rewritten in independent form. However, because it is believed that independent claims 1 and 7 are allowable, it is submitted that claims 5, 6, 11, and 12 are allowable in their current dependent form.

Conclusion:

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check or credit card payment form being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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